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1 The case for a configure-and-execute paradigm
Frank Vahid, Tony Givargis
March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign**
Publisher: ACM Press
Full text available: pdf(484.64 KB) Additional Information: full citation, references, citings, index terms

Keywords: IP, cores, methodology, system-on-a-chip

2 Hardware/software co-simulation in a VHDL-based test bench approach
Matthias Bauer, Wolfgang Ecker
June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**
Publisher: ACM Press
Full text available: pdf(88.32 KB) Additional Information: full citation, abstract, references, citings, index terms
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Novel test bench techniques are required to cope with afunctional test complexity which is predicted to grow muchmore strongly than design complexity. Our test benchapproach attacks this complexity by using a stronghierarchical architecture, application domain-independentsynchronization, reusable modules, and easy incrementalextendability based on table-driven techniques. In addition,the integration of VHDL/C co-simulation under the controlof the test bench makes it possible to use the hardware ...

3 Development of processors and communication networks for embedded systems: Component-based design approach for multicore SoCs
W. Cesário, A. Baghdadi, L. Gauthier, D. Lyonnard, G. Nicolescu, Y. Paviot, S. Yoo, A. A. Jerraya, M. Diaz-Nava
June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(187.82 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a high-level component-based methodology and design environment for application-specific multicore SoC architectures. Component-based design provides primitives to build complex architectures from basic components. This bottom-up approach allows design-architects to explore efficient custom solutions with best performances. This paper presents a high-level component-based methodology and design environment for application-specific multicore SoC architectures. The system speci ...

Keywords: HW/SW interfaces abstraction, component-based design, multicore System-on-Chip

4 Session 9B: communication architectures design and analysis: Efficient exploration of the SoC communication architecture design space

Kanishka Lahiri, Anand Raghunathan, Sujit Dey

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(171.27 KB) Additional Information: full citation, abstract, references, citings

In this paper, we present a methodology and efficient algorithms for the design of high-performance system-on-chip communication architectures. Our methodology automatically and optimally maps the various communications between system components onto a target communication architecture template that can consist of an arbitrary interconnection of shared or dedicated channels. In addition, our techniques simultaneously configure the communication protocols of each channel in the architecture in or ...

5 Prefetching for improved bus wrapper performance in cores

Roman Lysecky, Frank Vahid

January 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 1

Publisher: ACM Press

Full text available: pdf(430.83 KB) Additional Information: full citation, abstract, references, citings, index terms

Reuse of cores can reduce design time for systems-on-a-chip. Such reuse is dependent on being able to easily interface a core to any bus. To enable such interfacing, many propose separating a core's interface from its internals by using a bus wrapper. However, this separation can lead to a performance penalty when reading a core's internal registers. In this paper, we introduce prefetching, which is analogous to caching, as a technique to reduce or eliminate this performance penalty, involving a ...

Keywords: Bus wrapper, PVCI, VSIA, cores, design reuse, intellectual property, interfacing, on-chip bus, system-on-a-chip

6 Cosimulation of real-time control systems

Juha-Pekka Soininen, Tuomo Huttunen, Kari Tiensyrjä, Hannu Heusala

December 1995 **Proceedings of the conference on European design automation**

Publisher: IEEE Computer Society Press

Full text available: pdf(592.97 KB) Additional Information: full citation, references, citings, index terms

7 MILAN: A Model Based Integrated Simulation Framework for Design of Embedded Systems

A. Bakshi, V. K. Prasanna, A. Ledeczi

August 2001 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN workshop on Languages, compilers and tools for embedded systems LCTES '01 , Proceedings of the 2001 ACM SIGPLAN workshop on Optimization of middleware and distributed systems OM '01**, Volume 36 Issue 8

Publisher: ACM Press

Full text available: pdf(151.32 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We present MILAN, a model based extensible framework that facilitates rapid, multigranular performance evaluation of a large class of embedded systems, by seamlessly integrating different widely used simulators in to a unified environment. MILAN provides a formal paradigm for specification of structural and behavioral aspects of embedded systems, an integrated model-based approach, and a unified software environment for system design and simulation. This paper provides an overview of MILAN, d ...

8 Session 10B: Power saving techniques for embedded processors: A methodology for the design of application specific instruction set processors (ASIP) using the machine description language LISA

Andreas Hoffmann, Oliver Schliebusch, Achim Nohl, Gunnar Braun, Oliver Wahlen, Heinrich Meyr

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press
Full text available: pdf(913.02 KB) Additional Information: full citation, abstract, references, citings, index terms

The development of application specific instruction set processors (ASIP) is currently the exclusive domain of the semiconductor houses and core vendors. This is due to the fact that building such an architecture is a difficult task that requires expertise knowledge in different domains: application software development tools, processor hardware implementation, and system integration and verification. This paper presents a retargetable framework for ASIP design which is based on machine descript ...

9 Automatic generation of application-specific architectures for heterogeneous multiprocessor system-on-chip
Damien Lyonnard, Sungjoo Yoo, Amer Baghdadi, Ahmed A. Jerraya
June 2001 **Proceedings of the 38th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(285.15 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a design flow for the generation of application-specific multiprocessor architectures. In the flow, architectural parameters are first extracted from a high-level system specification. Parameters are used to instantiate architectural components, such as processors, memory modules and communication networks. The flow includes the automatic generation of communication coprocessor that adapts the processor to the communication network in an application-specific way. Experiments with ...

10 System partitioning and timing analysis: Transformation of SDL specifications for system-level timing analysis
Marek Jersak, Kai Richter, Rafik Henia, Rolf Ernst, Frank Slomka
May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**
Publisher: ACM Press
Full text available: pdf(539.27 KB) Additional Information: full citation, abstract, references, citings, index terms

Complex embedded systems are typically specified using multiple domain-specific languages. After code-generation, the implementation is simulated and tested. Validation of non-functional properties, in particular timing, remains a problem because full test coverage cannot be achieved for realistic designs. The alternative, formal timing analysis, requires a system representation based on key application and architecture properties. These properties must first be extracted from a system specifica ...

11 How application/technology evolutions will shape classical EDA?: System-on-chip beyond the nanometer wall
Philippe Magarshack, Pierre G. Paulin
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(454.87 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we analyze the emerging trends in the design of complex Systems-on-a-Chip for nanometer-scale semiconductor technologies and their impact on design automation requirements, from the perspective of a broad range SoC supplier.We present our vision of some of the key changes that will emerge in the next five years. This vision is characterized by two major paradigm changes. The first is that SoC design will become divided into four mostly non-overlapping distinct abstraction levels. ...

Keywords: design automation tools, embedded software technologies, multi-processor systems, network-on-chip, reconfigurable systems, system-on-chip

12 Automated Bus Generation for Multiprocessor SoC Design
Kyeong Keol Ryu, Vincent J. Mooney III
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**
Publisher: IEEE Computer Society
Full text available: pdf(197.20 KB) Additional Information: full citation, abstract, citings, index terms
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The performance of a system, especially a multiprocessor system, heavily depends upon the efficiency of its bus architecture. This paper presents a methodology to generate a

custom bus system for a multiprocessor System-on-a-Chip (SoC). Our bus synthesis tool (BusSyn) uses this methodology to generate five different bus systems as examples: Bi-FIFO Bus Architecture (BFBA), Global Bus Architecture Version I (GBAVI), Global Bus Architecture Version III (GBAVIII), Hybrid bus architecture (Hybrid) a ...

13 A Mixed Abstraction Level Co-Simulation Case Study Using SystemC for System on Chip Verification

Ali Sayinta, Gorkem Canverdi, Marc Pauwels, Amer Alshawa, Wim Dehaene

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2 DATE '03**

Publisher: IEEE Computer Society

Full text available: pdf(302.60 KB) Additional Information: full citation, abstract, index terms

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This paper focuses on co-simulation scenarios and their applications as a part of a system-on-chip (SoC) modeling and design methodology developed at Alcatel Microelectronics (now part of STMicroelectronics) within a wireless local area network (LAN) SoC project. This methodology proposes to build a SystemC-based executable model of the system to maintain a bridge between the algorithmic and the implementation worlds. The model is used in later phases by means of co-simulation of SystemC, HDL an ...

14 Efficient system exploration and synthesis of applications with dynamic data storage and intensive data transfer

Julio Leao da Silva, Chantal Ykman-Couvreur, Miguel Miranda, Kris Croes, Sven Wuytack, Gjalt de Jong, Francky Catthoor, Diederik Verkest, Paul Six, Hugo De Man

May 1998 **Proceedings of the 35th annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(241.06 KB) Additional Information: full citation, abstract, references, citings, index terms

Publisher Site

Matisse is a design flow intended for developing embedded systems characterize dby tight inter action b etwe encontrol and data-flow behavior, intensive data storage and tr ansfer, dynamic creation of data, and stringent real-time requirements. Matisse bridges the gap from a system specification, using a cocurr ent obje ct-oriented language, to an optimize d embedded single-chip HW/SW implementation. Matisse supp orts stepwise system-level exploration and refinement, memory architec ...

Keywords: PLA-style logic blocks, programmable logic devices, technology mapping

15 Emerging design and tool challenges in RF and wireless applications: 4G terminals: how are we going to design them?

Jan Craninckx, Stéphane Donnay

June 2003 **Proceedings of the 40th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(1.83 MB) Additional Information: full citation, abstract, references, index terms

Fourth-generation wireless communication systems (4G) will have totally different requirements than what front-end designers have been coping with up to now. Designs must be targeted to multi-mode and reconfigurability, leading to the concept of a "software-defined radio". A large part of such a radio will be integrated into a complex SoC, where the substrate noise coupling problem must be solved.However, for an optimal implementation of the complete system, including e.g. PA, RF filters and ant ...

Keywords: 4th generation, radio front-end, telecommunication, wireless systems

16 Operating system based software generation for systems-on-chip

Dirk Desmet, D. Verkest, Hugo De Man

June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(65.66 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we propose a system-level design environment, aimed at System-on-Chip (SOC) designs, including real-time embedded software. While many SOC modeling languages originate from hardware description languages, and thus tend to describe

statical architectures, we observe that embedded software makes SOC designs essentially dynamic, and so a SOC modeling environment must include dynamic behavior. Such behavior is analogous to the services an Operating System offers in the software wo ...

17 Modeling issues in the design of embedded systems: Architecture-level performance evaluation of component-based embedded systems

Jeffry T. Russell, Margarida F. Jacome

June 2003 **Proceedings of the 40th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(215.86 KB) Additional Information: full citation, abstract, references, index terms

A static performance evaluation technique is proposed to support early, architecture-level design space exploration for component-based embedded systems. The novel contribution is the use of a designer-specified evaluation scenario to identify a characteristic subset of system functionality that serves as a context for a rapid performance evaluation between candidate architectures. Fidelity is demonstrated with a case study that compares performance estimates of several candidate architectures t ...

Keywords: architecture-level, component-based, design space exploration, embedded system, performance evaluation, scenario

18 Timing coverification of concurrent embedded real-time systems

Pao-Ann Hsiung

March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign**

Publisher: ACM Press

Full text available: pdf(486.35 KB) Additional Information: full citation, references, citings, index terms

19 Co-design architecture and synthesis: A novel codesign approach based on distributed virtual machines

Christian Kreiner, Christian Steger, Egon Teiniker, Reinhold Weiss

May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**

Publisher: ACM Press

Full text available: pdf(541.82 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a hardware/software codesign approach for the design of embedded systems based on digital signal processors and FPGAs. Our approach is based on distributed virtual machines for simulation and verification of the application on a Linux cluster and for running the application on different target architectures (DSPs, FPGAs) as well. The main focus is the description of the virtual machine, which was designed to make DSP applications portable across different platforms while mai ...

20 Testbench, verification and debugging: practical considerations: Re-use-centric architecture for a fully accelerated testbench environment

Renate Henftling, Andreas Zinn, Matthias Bauer, Martin Zambaldi, Wolfgang Ecker

June 2003 **Proceedings of the 40th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(164.16 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a new technology that accelerates functional system verification. Starting with a behavioral testbench, we developed a seamless flow to generate a re-use-oriented architecture for a synthesizable testbench without loosing compatibility towith the original testbench. Consequently, we combine the flexibility of a behavioral testbench and the simulation performance of a synthesizable testbench, while greatly reducing the modeling overhead.The approach itself is hardware independ ...

Keywords: acceleration, functional verification, hardware testbench

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1. **System-level performance analysis for designing on-chip communication**
Lahiri, K.; Raghunathan, A.; Dey, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 20, Issue 6, June 2001 Page(s):768 - 783
Digital Object Identifier 10.1109/43.924830
AbstractPlus | References | Full Text: PDF(352 KB) **IEEE JNL**
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2. **SPI - a system model for heterogeneously specified embedded systems**
Ziegenbein, D.; Richter, K.; Ernst, R.; Thiele, L.; Teich, J.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 10, Issue 4, Aug. 2002 Page(s):379 - 389
Digital Object Identifier 10.1109/TVLSI.2002.807767
AbstractPlus | References | Full Text: PDF(823 KB) **IEEE JNL**
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3. **Hardware/software codesign of embedded systems the SPI workbench**
Ernst, R.; Ziegenbein, D.; Richter, K.; Thiele, L.; Teich, J.;
VLSI '99. Proceedings IEEE Computer Society Workshop On
8-9 April 1999 Page(s):9 - 17
Digital Object Identifier 10.1109/IWV.1999.760458
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4. **Efficient system exploration and synthesis of applications with dynamic i intensive data transfer**
Leao da Silva, J., Jr.; Chantal Ykman-Couvreur; Miranda, M.; Croes, K.; Wuyts G.; Catthour, F.; Verkest, D.; Six, P.; De Man, H.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):76 - 81
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11279911	Not Issued	19	01/01/0001	METHOD FOR MODELING METASTABILITY DECAY USING FENCE LOGIC INSERTION	SCHUPPE, RAYMOND W.
11149484	Not Issued	20	06/09/2005	Method, apparatus, and computer program product for facilitating modeling of a combinatorial logic glitch at an asynchronous clock domain crossing	SCHUPPE, RAYMOND W.M.
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